This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-27 (canceled)

Claim 28 (currently amended): A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes, each boost unit having input and output portions;

a first transistor connected between the input node and a node for receiving a first voltage;

a first capacitor having a first end which is connected to the output node, and a second end which receives a first oscillation signal;

a second transistor included in each boost unit;

a second capacitor included in each boost unit and connected to said input portion thereof; and

a third transistor connected to said output node, being unconnected to a gate of said first transistor,

wherein both a drain and a gate of said second transistor are connected to said input portion, a source of said second transistor is connected to said output portion, and said gate of said first transistor is connected to the input portion of one of said boost units, and when said third transistor ~~turns on and~~ transfers a second voltage from a source of said third transistor to a drain of said third transistor ~~without a voltage drop~~, ~~said first transistor turns off and~~ said voltage generating/transferring circuit becomes disabled, and as long as said third transistor transfers said second voltage, said third transistor is on.

Claim 29 (previously presented): The voltage generating/transferring circuit according to claim 28, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a fourth voltage of the gate of said fourth transistor is greater than or equal to a sum of said third voltage and a threshold voltage of said fourth transistor.

Claim 30 (previously presented): The voltage generating/transferring circuit according to claim 28, wherein a second oscillation signal is input to an even-numbered boost unit from the input node, a third oscillation signal is input to an odd-numbered boost unit from the input node, and the second and the third oscillation signals have opposite phases or different timings.

Claim 31 (previously presented): The voltage generating/transferring circuit according to claim 28, wherein gate and source voltage levels of said first transistor gradually rise while changing in opposite phases.

Claim 32 (previously presented): The voltage generating/transferring circuit according to claim 28, wherein the second voltage is 0V.

Claim 33 (previously presented): The voltage generating/transferring circuit according to claim 28, wherein a threshold voltage of said second transistor in at least one of the boost units is lower than a threshold voltage of said first transistor.

Claim 34 (currently amended): The voltage generating/transferring circuit according to claim ~~28~~33, wherein a threshold voltage of said second transistor in a boost unit closest to said output node is lower than a threshold voltage of said first transistor.

Claim 35 (previously presented): The voltage generating/transferring circuit according to claim 28, wherein a threshold voltage of said second transistor in a boost unit on the output node side is lower than a threshold voltage of said second transistor in a boost unit on the input node side.

Claim 36 (previously presented): The voltage generating/transferring circuit according to claim 28, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a fourth voltage of the gate of said fourth transistor is greater than or equal to a sum of the third voltage and a threshold voltage of said fourth transistor in transferring the third voltage.

Claim 37 (currently amended): The voltage generating/transferring circuit according to claim 28, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

a fifth transistor connected to ~~a~~ said gate of said ~~fourth~~ first transistor,

wherein when said fifth transistor turns on and transfers a fourth voltage from a source of said fifth transistor to a drain of said fifth transistor ~~without a voltage drop~~, said ~~fourth~~ first transistor turns off and said voltage generating/transferring circuit becomes disabled.

Claim 38 (previously presented): The voltage generating/transferring circuit according to claim 37, wherein the fourth voltage is 0V.

Claim 39 (currently amended): The voltage generating/transferring circuit according to claim 28, further comprising:

a fourth transistor connected to said ~~output node~~gate of said first transistor,

wherein when said fourth transistor turns on and transfers a third voltage from a source of said fourth transistor to a drain of said fourth transistor ~~without a voltage drop~~, said voltage generating/transferring circuit becomes disabled.

Claim 40 (previously presented): The voltage generating/transferring circuit according to claim 28, wherein the first oscillation signal and a second oscillation signal which is input to the boost unit connected to the first capacitor have opposite phases or different timings.

Claim 41 (previously presented): The voltage generating/transferring circuit according to claim 28, wherein a threshold voltage of the second transistor is lower than a threshold voltage of the first transistor.

Claim 42 (currently amended): A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes, each boost unit having input and output portions;

a first transistor connected between the input node and a node for receiving a first voltage;

a first capacitor having a first end which is connected to the output node, and a second end which receives a first oscillation signal;

a second transistor included in each boost unit;

a second capacitor included in each boost unit and connected to said input portion thereof; and

a third transistor connected to <u>said output node, being unconnected to</u> a gate of said first transistor,

wherein both a drain and a gate of said second transistor are connected to said input portion, a source of said second transistor is connected to said output portion, and said gate of said first transistor is connected to the input portion of one of said boost units, a charge moves between the output portion of one of the boost units and the input portion of another of the boost units, and when said third transistor ~~turns on and~~ transfers a second voltage from a source of said third transistor to a drain of said third transistor ~~without a voltage drop, said first transistor turns off and~~ said voltage generating/transferring circuit becomes disabled, <u>and as long as said third transistor transfers said second voltage, said third transistor is on</u>.

Claim 43 (previously presented): The voltage generating/transferring circuit according to claim 42, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a fourth voltage of the gate of said fourth transistor is greater than or equal to a sum of the third voltage and a threshold voltage of said fourth transistor.

Claim 44 (previously presented): The voltage generating/transferring circuit according to claim 42, wherein a second oscillation signal is input to an even-numbered boost unit from the input node, a third oscillation signal is input to an odd-numbered boost unit from the input node, and the second and the third oscillation signals have opposite phases or different timings.

Claim 45 (previously presented): The voltage generating/transferring circuit according to claim 42, wherein gate and source voltage levels of said first transistor gradually rise while changing in opposite phases.

Claim 46 (previously presented): The voltage generating/transferring circuit according to claim 42, wherein the second voltage is 0V.

Claim 47 (previously presented): The voltage generating/transferring circuit according to claim 42, wherein a threshold voltage of said second transistor in at least one of the boost units is lower than a threshold voltage of said first transistor.

Claim 48 (previously presented): The voltage generating/transferring circuit according to claim 42, wherein a threshold voltage of said second transistor in a boost unit closest to said output node is lower than a threshold voltage of said first transistor.

Claim 49 (previously presented): The voltage generating/transferring circuit according to claim 42, wherein a threshold voltage of said second transistor in a boost unit on the output node side is lower than a threshold voltage of said second transistor in a boost unit on the input node side.

Claim 50 (previously presented): The voltage generating/transferring circuit according to claim 42, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a fourth voltage of the gate of said fourth transistor is greater than or equal to a sum of the third voltage and a threshold voltage of said fourth transistor in transferring the third voltage.

Claim 51 (currently amended): The voltage generating/transferring circuit according to claim 42, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

a fifth transistor connected to ~~a~~ said gate of said ~~fourth~~ first transistor,

wherein when said fifth transistor turns on and transfers a fourth voltage from a source of said fifth transistor to a drain of said fifth transistor ~~without a voltage drop~~, said ~~fourth~~ first transistor turns off and said voltage generating/transferring circuit becomes disabled.

Claim 52 (previously presented): The voltage generating/transferring circuit according to claim 51, wherein the fourth voltage is 0V.

Claim 53 (currently amended): The voltage generating/transferring circuit according to claim 42, further comprising:

a fourth transistor connected to said ~~output node~~gate of said first transistor,

wherein when said fourth transistor turns on and transfers a third voltage from a source of said fourth transistor to a drain of said fourth transistor ~~without a voltage drop~~, said voltage generating/transferring circuit becomes disabled.

Claim 54 (previously presented): The voltage generating/transferring circuit according to claim 42, wherein the first oscillation signal and a second oscillation signal which is input to the boost unit connected to the first capacitor have opposite phases or different timings.

Claim 55 (previously presented): The voltage generating/transferring circuit according to claim 42, wherein a threshold voltage of the second transistor is lower than a threshold voltage of the first transistor.

Claim 56 (currently amended): A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes directly, each boost unit having input and output portions;

a first transistor connected between the input node and a node for receiving a first voltage;

a first capacitor having a first end which is connected to the output node, and a second end which receives a first oscillation signal;

a second transistor included in each boost unit;

a second capacitor included in each boost unit and connected to said input portion thereof; and

a third transistor connected to said output node, being unconnected to a gate of said first transistor,

wherein both a drain and a gate of said second transistor are connected to said input portion, a source of said second transistor is connected to said output portion, and said gate of said first transistor is connected to the input portion of one of said boost units, and when said third transistor ~~turns on and~~ transfers a second voltage from a source of said third transistor to a drain of said third transistor ~~without a voltage drop, said first transistor turns off and~~ said voltage generating/transferring circuit becomes disabled, and as long as said third transistor transfers said second voltage, said third transistor is on.

Claim 57 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein a source or a drain of said first transistor is directly connected to the input node.

Claim 58 (previously presented): The voltage generating/transferring circuit according to claim 56, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a fourth voltage of the gate of said fourth transistor is greater than or equal to a sum of the third voltage and a threshold voltage of said fourth transistor.

Claim 59 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein a second oscillation signal is input to an even-numbered boost unit from the input node, a third oscillation signal is input to an odd-numbered boost unit from the input node, and the second and the third oscillation signals have opposite phases or different timings.

Claim 60 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein gate and source voltage levels of said first transistor gradually rise while changing in opposite phases.

Claim 61 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein the second voltage is 0V.

Claim 62 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein a threshold voltage of said second transistor in at least one of the boost units is lower than a threshold voltage of said first transistor.

Claim 63 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein a threshold voltage of said second transistor in a boost unit closest to said output node is lower than a threshold voltage of said first transistor.

Claim 64 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein a threshold voltage of said second transistor in a boost unit on the output node side is lower than a threshold voltage of said second transistor in a boost unit on the input node side.

Claim 65 (previously presented): The voltage generating/transferring circuit according to claim 56, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a fourth voltage of the gate of said fourth transistor is greater than or equal to a sum of said third voltage and a threshold voltage of said fourth transistor in transferring the third voltage.

Claim 66 (currently amended): The voltage generating/transferring circuit according to claim 56, further comprising:

a fourth transistor which has a gate connected to the output node, and transfers a third voltage,

a fifth transistor connected to ~~a~~ said gate of said ~~fourth~~ first transistor,

wherein when said fifth transistor turns on and transfers a fourth voltage from a source of said fifth transistor to a drain of said fifth transistor ~~without a voltage drop~~, said ~~fourth~~ first transistor turns off and said voltage generating/transferring circuit becomes disabled.

Claim 67 (previously presented): The voltage generating/transferring circuit according to claim 66, wherein the fourth voltage is 0V.

Claim 68 (currently amended): The voltage generating/transferring circuit according to claim 56, further comprising:

a fourth transistor connected to said ~~output node~~ gate of said first transistor,

wherein when said fourth transistor turns on and transfers a third voltage from a source of said fourth transistor to a drain of said fourth transistor ~~without a voltage drop~~, said voltage generating/transferring circuit becomes disabled.

Claim 69 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein the first oscillation signal and a second oscillation signal which is input to the boost unit connected to the first capacitor have opposite phases or different timings.

Claim 70 (previously presented): The voltage generating/transferring circuit according to claim 56, wherein a threshold voltage of the second transistor is lower than a threshold voltage of the first transistor.

Claim 71 (new): A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes, each boost unit having input and output portions;

a first transistor connected between the input node and a node for receiving a first voltage;

a first capacitor having one end which is connected to the output node, and another end which receives a first oscillation signal;

a second transistor included in each boost unit;

a second capacitor included in each boost unit and connected to said input portion;

a third transistor connected to said output node, being unconnected to a gate of said first transistor; and

a fourth transistor connected to said gate of said first transistor,

wherein both a drain and a gate of said second transistor are connected to said input portion, a source of said second transistor is connected to said output portion, and said gate of said first transistor is connected to the input portion of one of said boost units, and when said third transistor transfers a second voltage from a source of said third transistor to a drain of said third transistor said voltage and said fourth transistor transfers a third voltage from a source of said fourth transistor to a drain of said fourth transistor, the generating/transferring circuit becomes disabled, and as long as said third transistor transfers said second voltage and said fourth transistor transfers said third voltage, said third transistor and said fourth transistor are on.

Claim 72 (new): A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes, each boost unit having input and output portions;

a first transistor connected between the input node and a node for receiving a first voltage;

a first capacitor having one end which is connected to the output node, and another end which receives a first oscillation signal;

a second transistor included in each boost unit;

a second capacitor included in each boost unit and connected to said input portion;

a third transistor connected to said output node, being unconnected to a gate of said first transistor; and

a fourth transistor connected to said gate of said first transistor,

wherein both a drain and a gate of said second transistor are connected to said input portion, a source of said second transistor is connected to said output portion, and said gate of said first transistor is connected to the input portion of one of said boost units, a charge moves between the output portion of one of the boost units and the input portion of another of the boost units, and when said third transistor transfers a second voltage from a source of said third transistor to a drain of said third transistor said voltage and said fourth transistor transfers a third voltage from a source of said fourth transistor to a drain of said fourth transistor, the generating/transferring circuit becomes disabled, and as long as said third transistor transfers said second voltage and said fourth transistor transfers said third voltage, said third transistor and said fourth transistor are on.

Claim 73 (new): A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes directly, each boost unit having input and output portions;

a first transistor connected between the input node and a node for receiving a first voltage;

a first capacitor having one end which is connected to the output node, and another end which receives a first oscillation signal;

a second transistor included in each boost unit;

a second capacitor included in each boost unit and connected to said input portion;

a third transistor connected to said output node, being unconnected to a gate of said first transistor; and

a fourth transistor connected to said gate of said first transistor,

wherein both a drain and a gate of said second transistor are connected to said input portion, a source of said second transistor is connected to said output portion, and said gate of said first transistor is connected to the input portion of one of said boost units, and when said third transistor transfers a second voltage from a source of said third transistor to a drain of said third transistor said voltage and said fourth transistor transfers a third voltage from a source of said fourth transistor to a drain of said fourth transistor, the generating/transferring circuit becomes disabled, and as long as said third transistor transfers said second voltage and said fourth transistor transfers said third voltage, said third transistor and said fourth transistor are on.